Pattern Transfer of Images Printed with Extreme Ultraviolet Lithography and Its Relevance to Device Fabrication.

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Presentation Outline

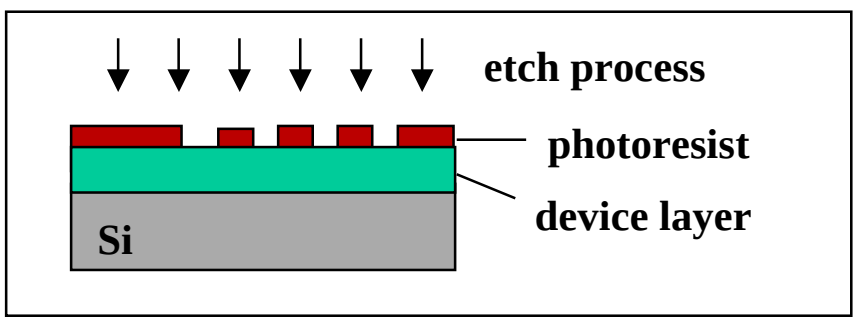
- **Background**
- **Description of Experiment**
- **Experimental Results**
- **Summary**

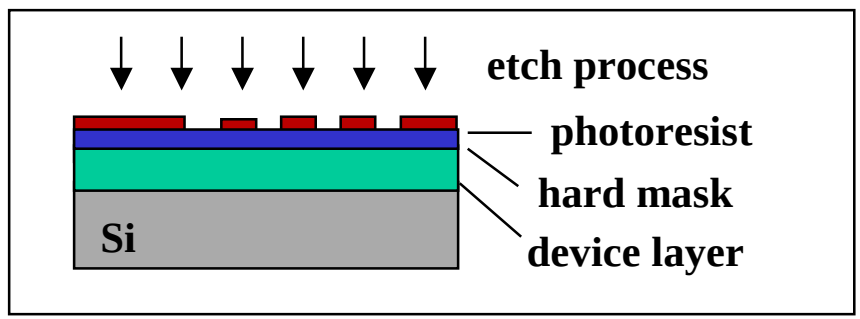
Thin Layer Photoresists May not have Sufficient Etch Resistance Required for Device Processing

- **Integrated circuit fabrication relies on pattern transfer using an etch process**
- **EUVL utilizes thin photoresist (typically ~ 100 nm thick).**
- **Thin photoresist must withstand etch processes during pattern transfer.**
- **Two approaches to improving ultimate etch resistance:**
  - **Intermediate hard-mask layer**
  - **Thicker resists (e.g., 175 nm)**

Can Thin Photoresist Layers Withstand Etching?

- **Initial concern: Thin resist (~ 100 nm) for pattern transfer may not have sufficient etch resistance or selectivity to layer etch, e.g., resist on polySi.**
- **One Approach: Use hard mask material such as SiO_2 or SiON, between the top resist layer and underlying silicon.**





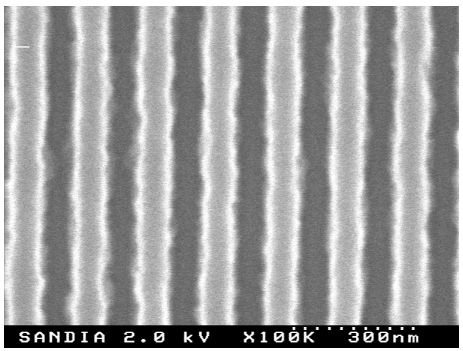
We Investigated Two Hard Mask Materials

- **Two hard mask-experiments:**
  - **Motorola's Advanced Products Research and Development Laboratory, Austin, TX.**
    - **Used SiO_2 and SiON hard mask layers on bare Si.**
  - **Microfabrication Facilities at UC Berkeley, Berkeley, CA.**
    - **Deposited low-temperature oxide (LTO) on polysilicon ("poly").**

- **Both Experiments Utilize EUVL for photoresist patterning.**

Sandia's 10x EUV Exposure Tool was used for all Top-Layer Imaging

- **Routinely achieve 70 nm resolution**

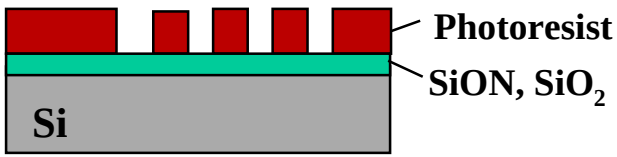


- **Schwarzschild design**
  - Spherical elements
  - WFE 0.05 waves rms
  - NA 0.088 - 0.1

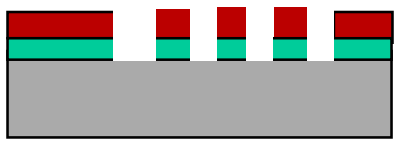
Motorola Process Utilizes Oxide and Nitride Hard Masks

Motorola Process

- Imaging layer patterned by EUVL



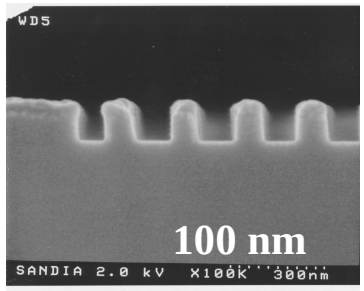
- Hard mask etch by RIE or ECR

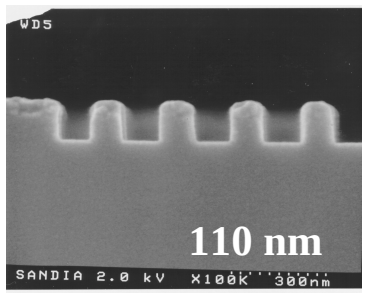


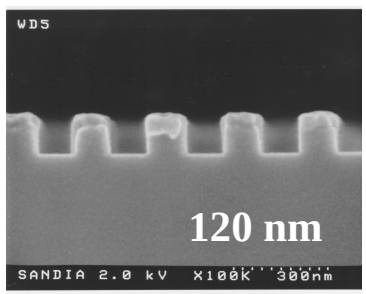
- **Hard mask Material :**
  - SiO_2 (87 nm)
  - SiON (50 nm)
- **Etch Process**
  - ECR
  - RIE
  - Halogen Gases

Hard Mask Results

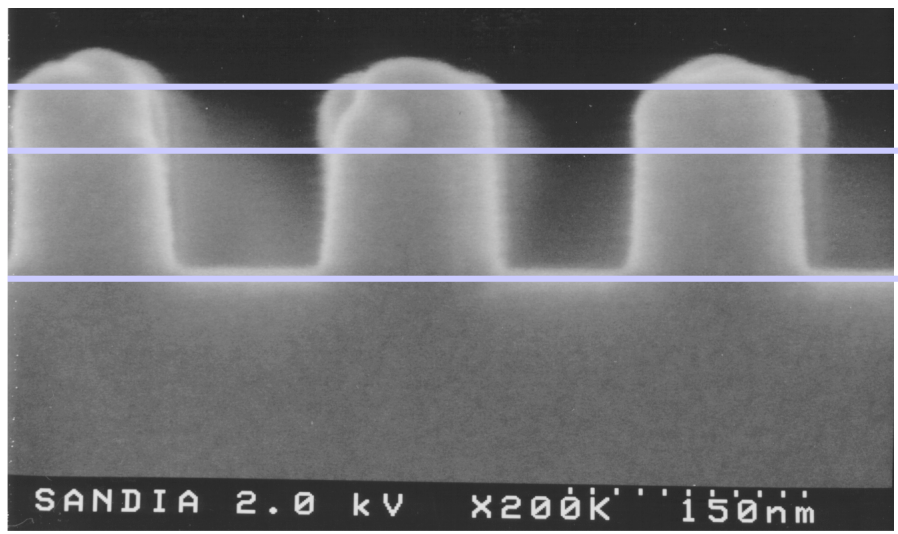
Motorola Process Demonstrates Pattern Transfer into SiO_2 Hard Mask







- **Remaining resist thickness is ~ 30 nm.**
- **Etch selectivity as great as 7:1**
- **Hard mask Sidewalls are ~85°.**

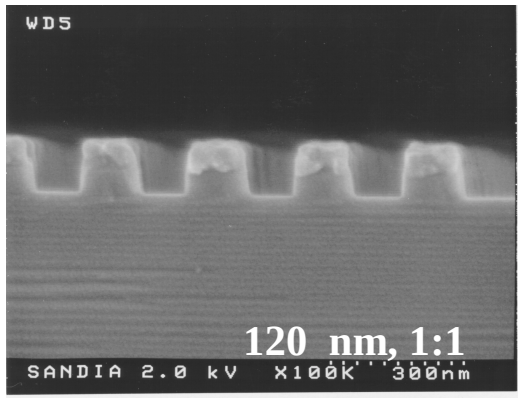


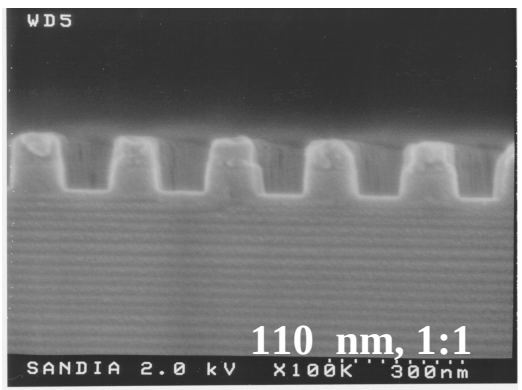
30 nm photoresist

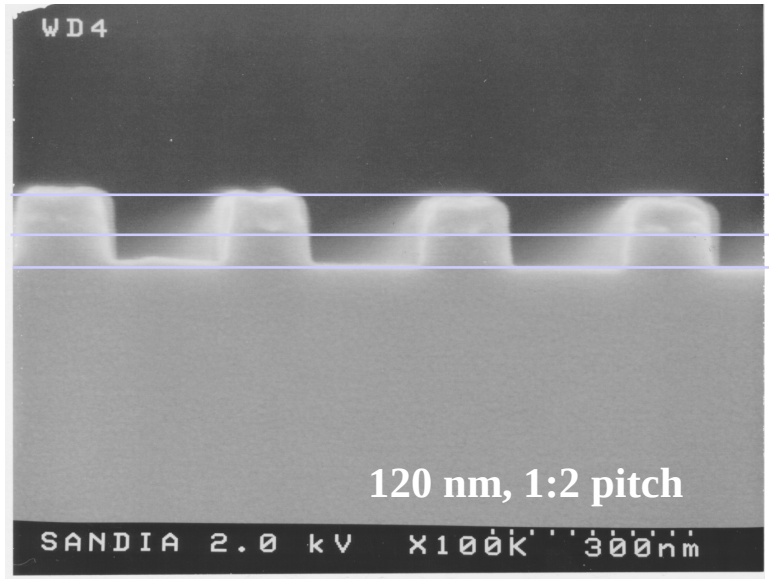
87 nm SiO_2 hard mask

SEM Micrographs of post-etch features

Excellent Results Achieved with SiON Hard Mask





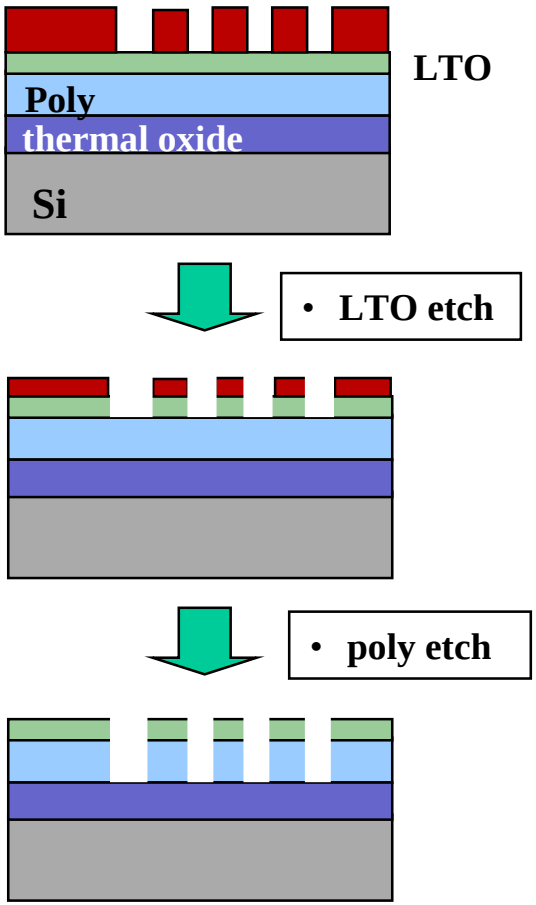


55 nm resist
50 nm SiON

Motorola Process demonstrates sufficient etch selectivity to accomplish pattern transfer into either SiO_2 or SiON hard masks.

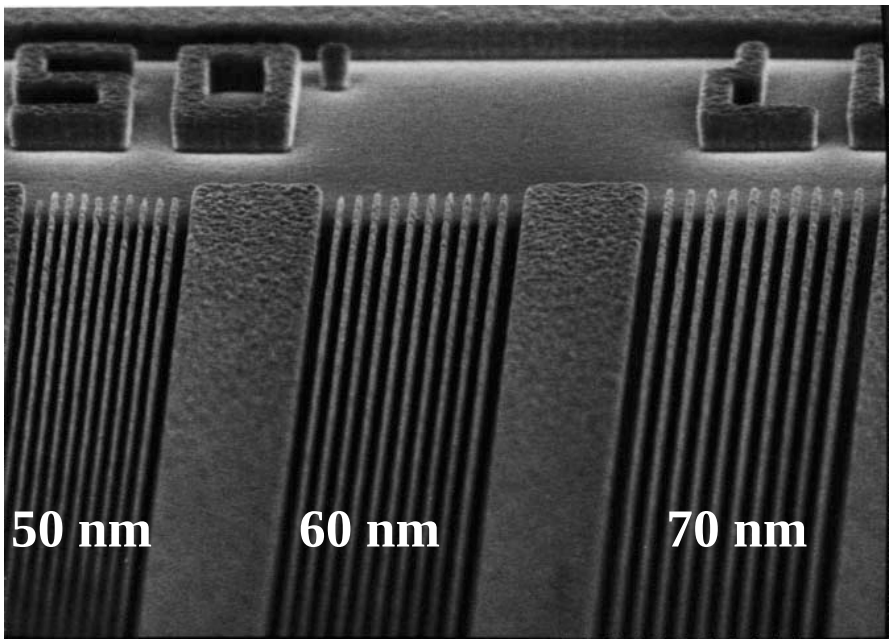
Sandia Hard Mask Utilizes a LTO Intermediate Layer

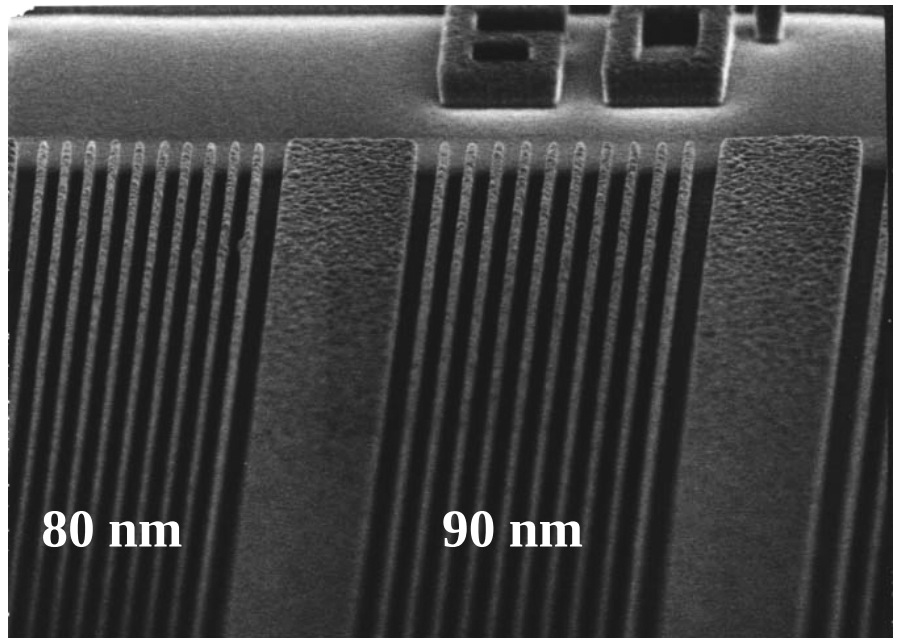
Sandia



- **Hard mask Material :**
  - **Low-temperature oxide (LTO), 50 - 60 nm.**
- **Polysilicon thickness = 350 nm**
- **Etch Process**
  - **Oxide Etch: RIE**
  - **Poly Etch: TCP**
  - **Oxide Etch: Ar, CF_4, CHF_3, 50 mTorr, 180W**
  - **Poly Etch: Cl_2 + HBr, 12 mTorr, 150W**
- **Thermal oxide used for endpoint detection.**

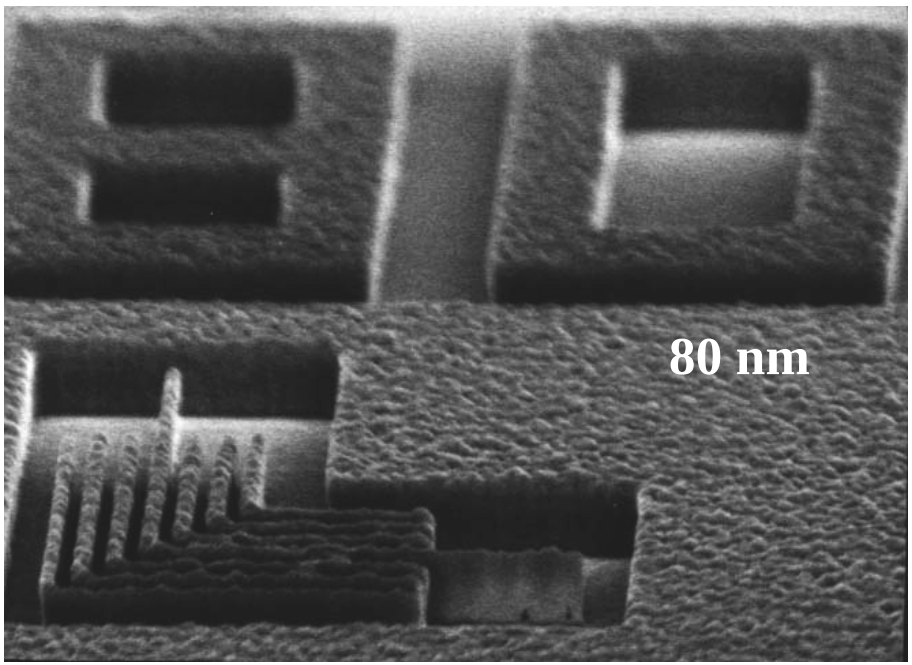
Pattern Transfer Through Polysilicon Demonstrated Using Sandia LTO Hard Mask Process

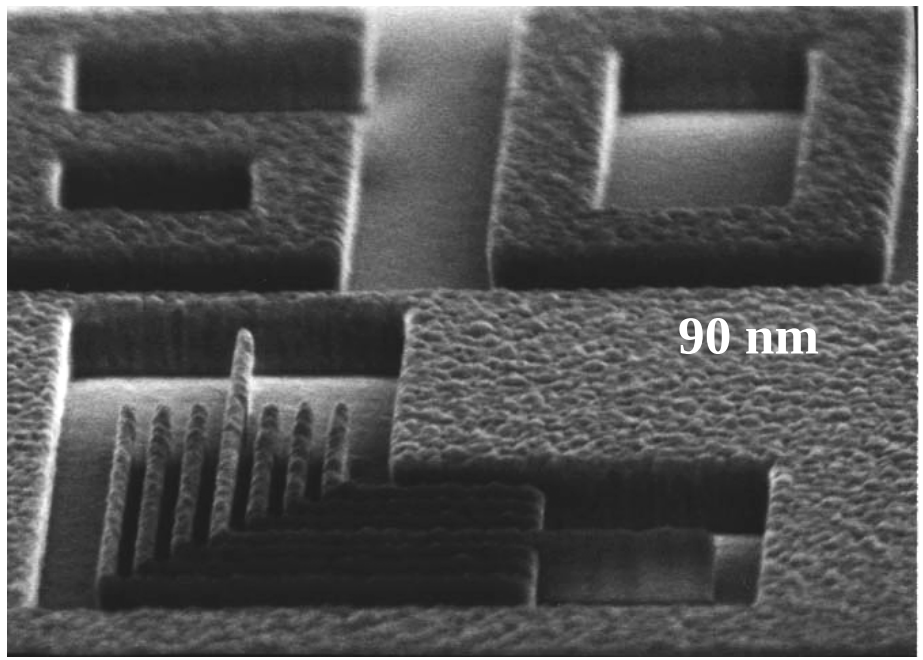




Pattern transfer in 1:2 pitch features as small as 50 nm (as-coded)

Pattern Transfer Facilitated by Improved Etch Selectivity



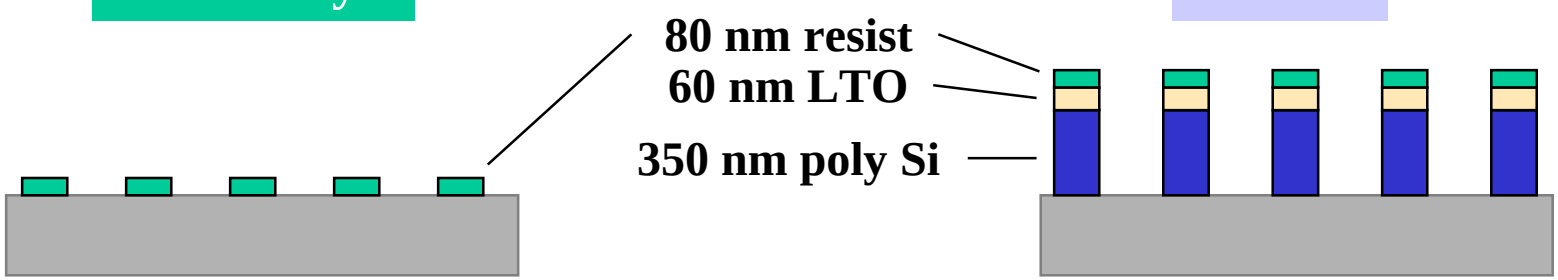


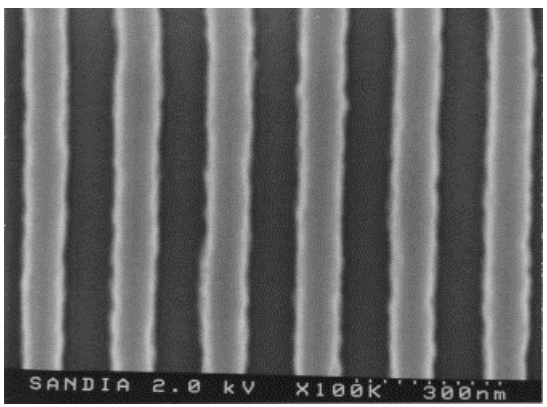
- **LTO / Photoresist selectivity ~ 3:1 (non-optimized).**
- **PolySi / LTO selectivity = > 10:1.**
- **Low Iso-dense bias**

Etched Features Exhibit Only Small Changes in LER

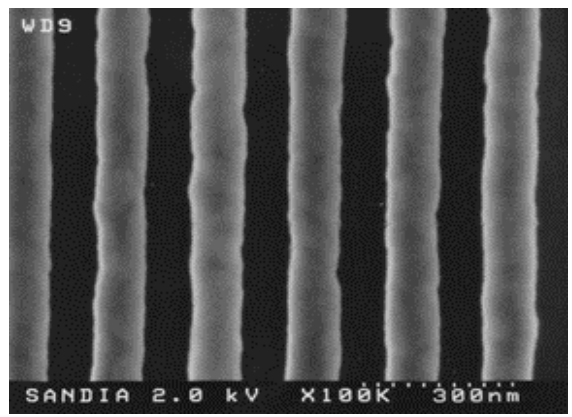
Resist only

Etched





100 nm (1:1)

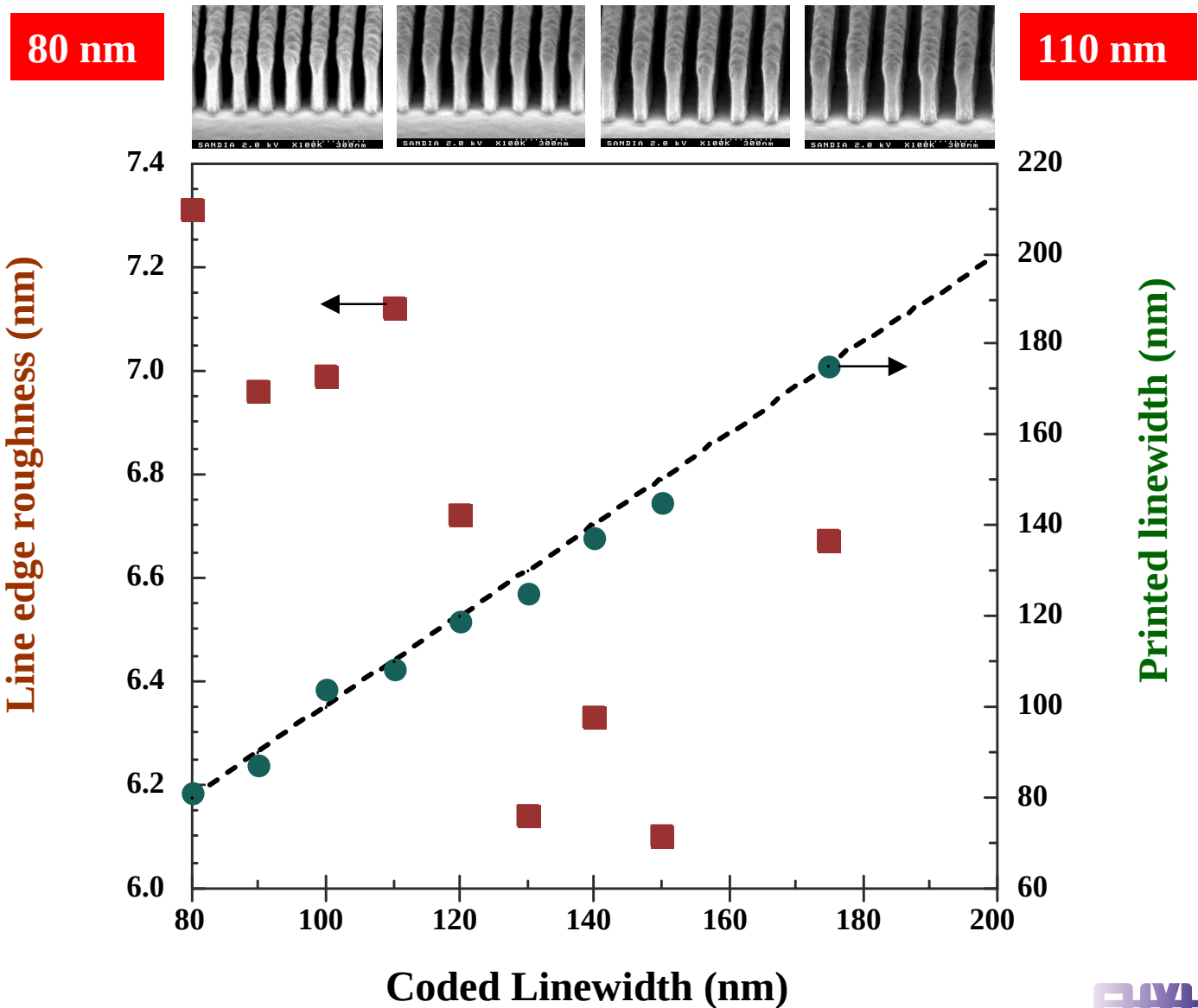


LER: 5.5 nm (3σ one side)

LER: 7.0 nm (3σ one side)

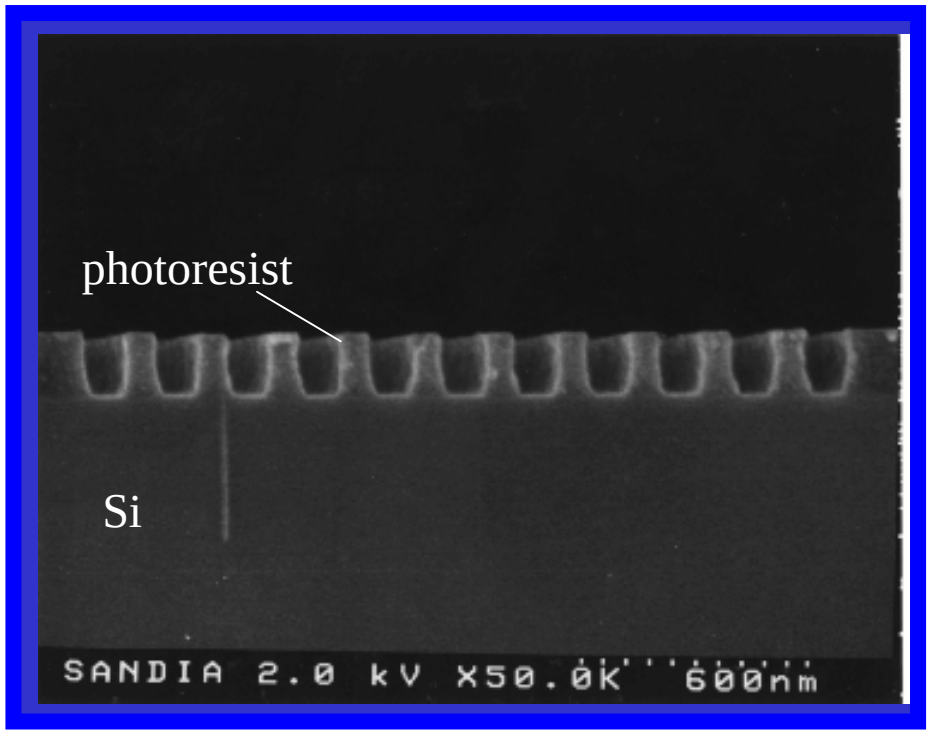
0.088NA

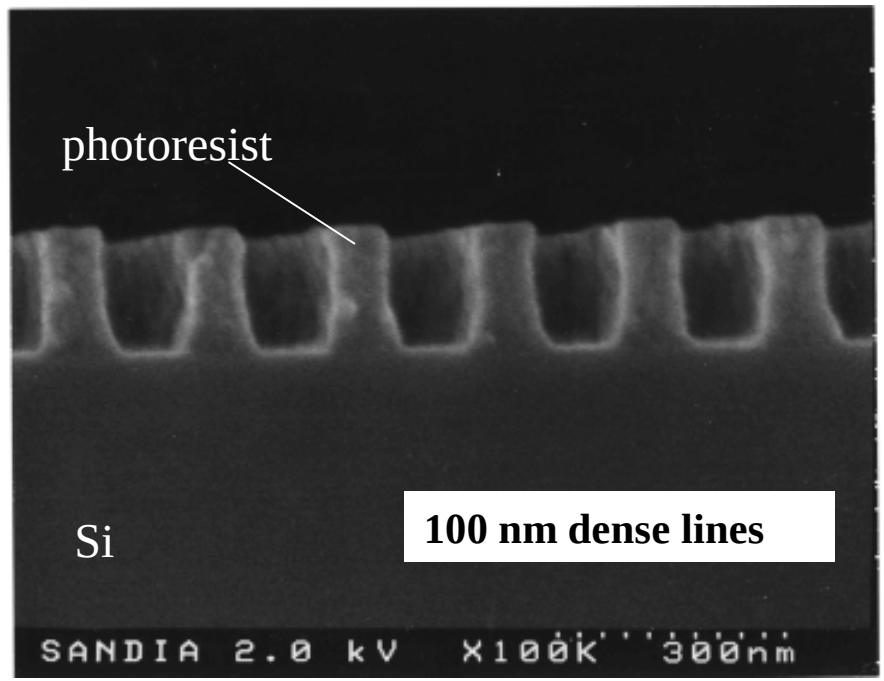
Etched Polysilicon Dense lines-and-spaces Exhibit Good Linearity and Low Line Edge Roughness



Single Layer, 175 nm Thick, Resist Results

Thick Resist Experimental Results: 100 nm L/S

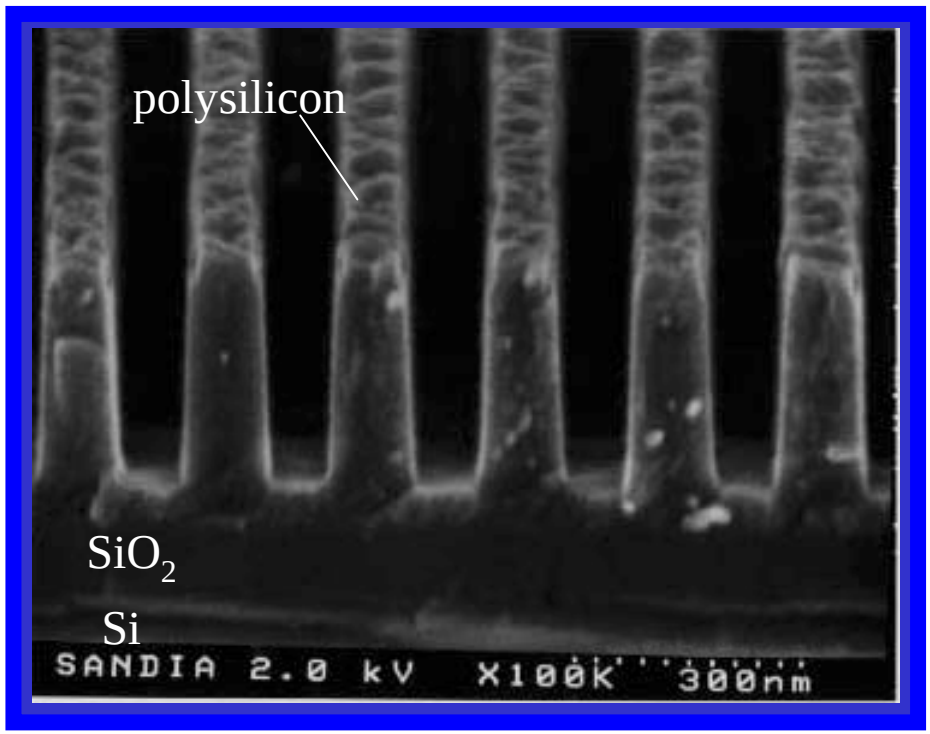


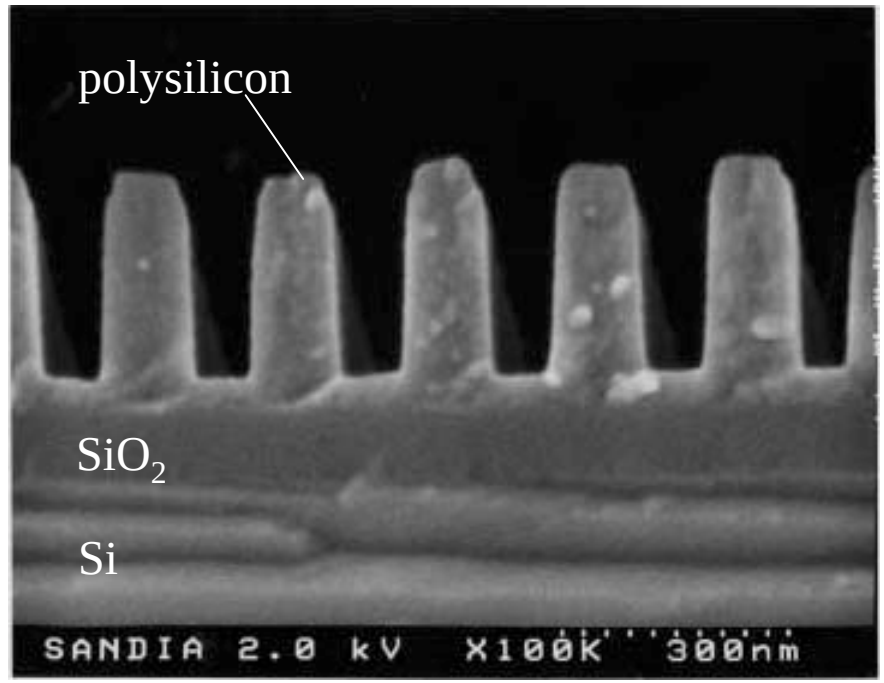


SEM Micrographs of printed photoresist on Si wafer.

- **100 nm dense lines/spaces**
- **175 nm thick resist**
- **1.3X Dose compared to 100 nm thick resist.**

Polysilicon Etch Using a Single Layer Resist Demonstrated





SEM Micrographs of etched polysilicon, 100 nm dense lines

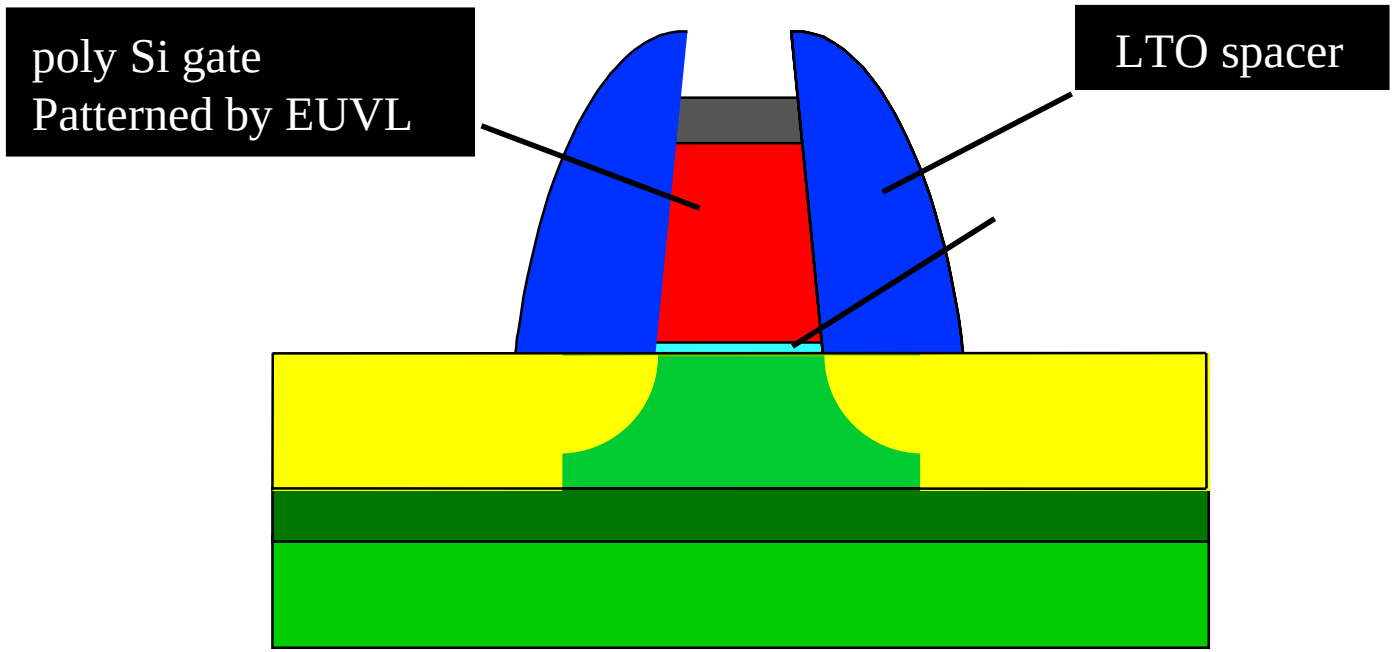
- **175 nm thick resist**
- **300 nm thick polysilicon after RIE etch**

MOSFET Device Fabrication Experiments

We Compare Polysilicon Gate Etching Using Two Pattern Transfer Processes

- **Use MOSFET device process flow…**
  - **Lightly-doped drain (LDD) n-channel MOSFET device**
  - **100 nm gate CD design rules**
  - **EUVL used for gate patterning (critical layer) and I-line litho for non-critical layers.**
- **Demonstrate pattern transfer into polysilicon gates in MOSFETs using two processes:**
  - **100 nm thick resist layer with LTO hard mask**
  - **Single layer resist, 175 nm thick.**
- **Compare Etch Results of two processes**

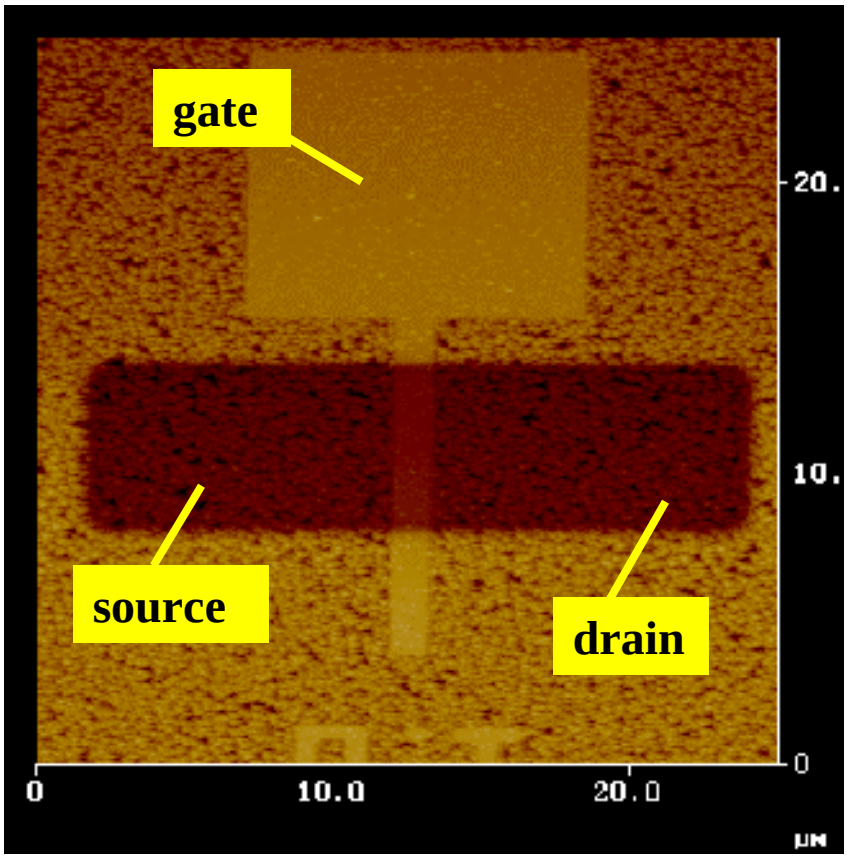
Cross-Section Illustration of EUVL Device



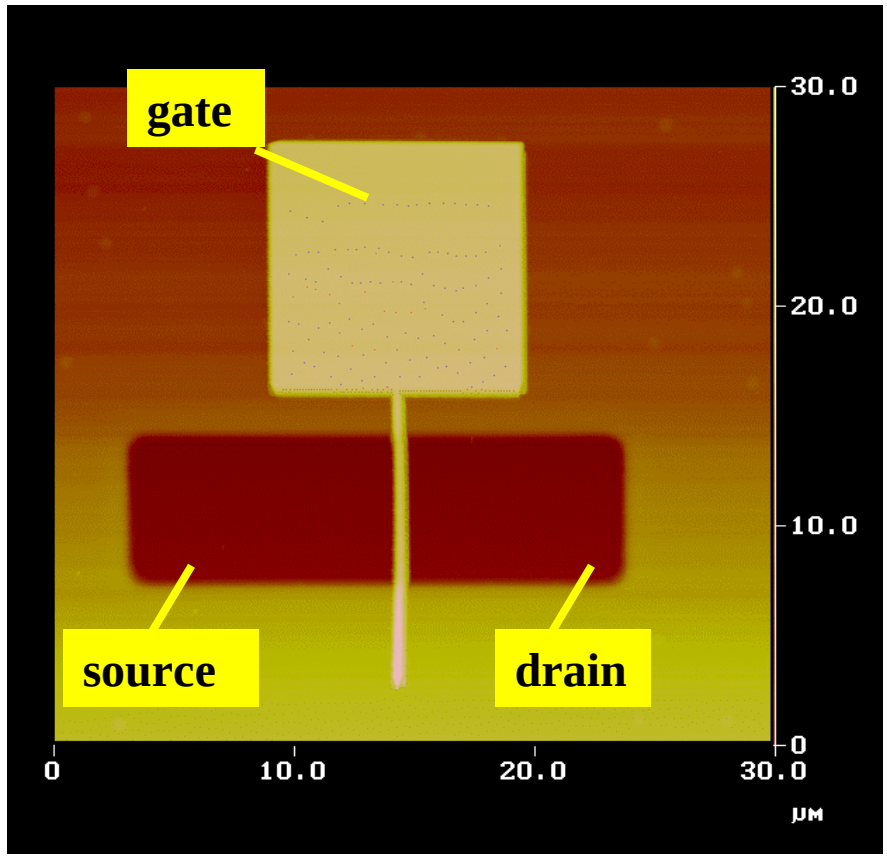
- EUVL patterning of gates at Sandia (10x-Microstepper).
- I-line for non-critical levels performed at UC Berkeley Microlab.
- Combines standard IC fabrication with EUVL to process MOSFET.

AFM Analysis Shows Less Roughness in Active Region Using 175 nm Resist Compared to LTO Hard Mask

LTO hard mask

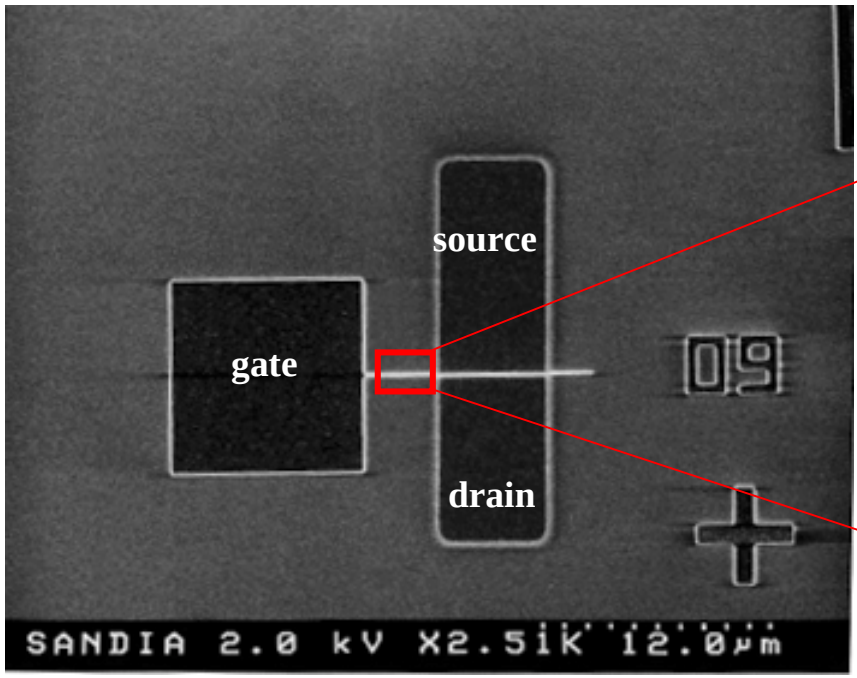


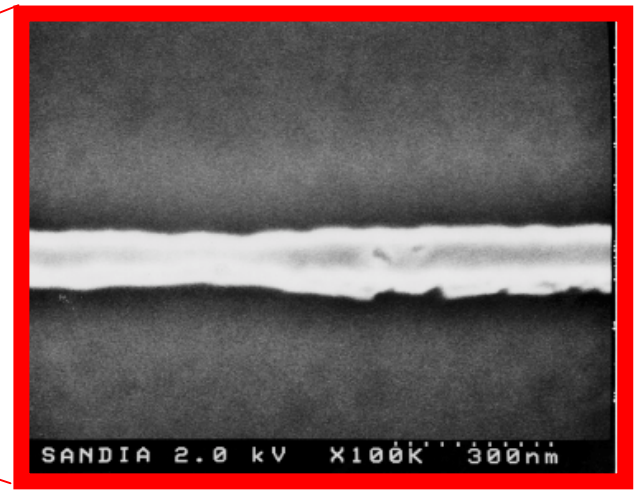
Single layer, no hard mask



- Substantial reduction of surface roughness in active region
  - **–3.5 X reduction in RMS roughness**
  - **–10X reduction in mean roughness (Ra)**

Thicker Photoresist and Optimized Etch Produces Improved MOSFET Gate Etch Results





- **SEM micrograph of 90 nm gate after poly etch**

- Simplified MOSFET Process Flow
  - **–No hard mask deposition, etch or strip (reduce by 3 steps).**

Summary

- **Pattern transfer using single layer resist with hard mask is feasible for IC processing.**

- **Thicker photoresist, i.e., 175 nm, without the use of a hard mask shows sufficient etch resistance for polySi gate processing.**

- **Using our LTO process, there is considerably less active region roughness after gate etch using the single-layer without hard mask process. This is likely due to defects (e.g., pinholes) in the LTO hard mask layer. However, LTO hard mask film process optimization would reduce the difference in post-etch roughness.**